Cont'd A1

6. (Amended) The fabricating method of claim 3, wherein the insulative material completely encapsulates the top surfaces and peripheries of the passive devices through a dispensing process.

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15. (Amended) The semiconductor package of claim 11, wherein the insulative material is a thermosetting or thermoplastic material selected from the group consisting of epoxy, silicone and polyimide.

A2

16. (Amended) The semiconductor package of claim 13, wherein the insulative material completely encapsulates the top surfaces and peripheries of the passive devices through a dispensing process.

REMARKS

Claims 1-20 are pending in the application. Claims 5, 6, 15, and 16 have been amended by the present amendment.

Attached hereto is a Letter to Official Draftsman with proposed drawing corrections. Specifically, in FIG. 4D, the lead line for reference numeral 52 has been shifted, and therefore it is now clear that reference numeral 52 refers to the entire **adhesive**, whereas reference numeral 40 points to the top surface of insulative material 4 (see specification at page 6, line 23 to page 7, line 2). It is respectfully requested that the drawing objections be withdrawn.

The following additional changes have been made to the drawings: in FIG. 3, reference numeral 1 has been added to indicate the semiconductor package (see specification at page 5, line 14), and reference numeral 222 has been added to indicate the solder pads (see specification at page 7, lines 13-17); in FIG. 4A, reference numerals for the device-mounting region 21 and solder pads 210 have been corrected (see specification at page 5, line 22 to page 6, line 3); in FIG. 4B, the lead line for reference numeral 210 has been corrected to indicate the entire solder pad; and in FIG. 4E, reference numerals have been added to indicate the bonding pads 500 and

bonding fingers 220 (see specification at page 7, lines 8-10). Approval of the drawing corrections is respectfully requested.

Claims 5 and 15 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Claims 5 and 15 have been amended to replace "such as" with "selected from the group consisting of," to indicate that the insulative material is a thermosetting or thermoplastic material selected from the group consisting of epoxy, silicone and polyimide. It is respectfully requested that the rejection under 35 USC 112 be withdrawn.

Claims 6 and 16 have been amended to clarify that the insulative material completely encapsulates the top surfaces and peripheries of the passive devices.

Applicants claim a semiconductor package and fabricating method, including: a substrate having a device-mounting region; a plurality of passive devices attached to the device-mounting region; an insulative material for encapsulating the passive devices; and a semiconductor chip disposed on a surface of the insulative material above the passive devices. The claimed method includes steps of: using an insulative material for encapsulating the passive devices, and disposing a semiconductor chip on a surface of the insulative material above the passive devices. Therefore, the claimed apparatus and method both require encapsulating the passive devices with an insulative material and disposing the semiconductor chip on a surface of the insulative material **above** the passive devices.

As shown in FIG. 3, a plurality of passive devices 3 are attached to a substrate 2 and encapsulated by an insulative material 4. The semiconductor chip 5 is mounted on the top surface of the insulative material 4 **above** the passive devices 3.

The above-described semiconductor package and fabricating method can yield significant benefits. Because the passive devices are vertically positioned under the semiconductor chip, they occupy a reduced area of the substrate (see specification at page 4, lines 13-15), as

compared to prior art packages in which passive devices are positioned beside a semiconductor chip. Moreover, as the passive devices are encapsulated before mounting of the semiconductor chip, direct contact between the passive devices and bonding wires is prevented, thereby eliminating the occurrence of short circuits (see specification at page 4, line 24 to page 5, line 2).

Claims 1-5, 7, 10-15, 17, and 20 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,355,283 to Marrs et al. (hereinafter "Marrs") in view of U.S. Patent 5,249,354 to Richman (hereinafter "Richman"). Claims 6, 8, 9, 16, 18, and 19 were rejected under 35 USC 103(a) as being unpatentable over "Marrs and Richman ... and further in view of" U.S. Patent 6,022,583 to Falcone et al. (hereinafter "Falcone"). These rejections are respectfully traversed, and for convenience are addressed together.

Marrs fails to teach or suggest a semiconductor package or fabricating method in which a plurality of passive devices are encapsulated and a semiconductor chip is disposed above the passive devices. In Marrs, one or more electronic devices (such as chips, passive components, etc.) are mounted on a substrate. A plurality of vias are formed through the substrate, and plated with electrically conductive material for interconnecting conductive traces on a surface of the substrate to solder ball pads on an opposite surface of the substrate.

With reference to the embodiment of FIG. 6 (cited in the Office Action), an integrated circuit chip 601 is attached to substrate 602, and vias 607 electrically connect traces 605 to the pads 608 on which solder balls 604 are formed (see column 7, lines 10-25). In Marrs, it is noted that "[p]assive components, such as resistors and capacitors, can also be mounted on the substrate" (column 2, lines 66-67). However, there is no teaching or suggestion in Marrs for disposing a semiconductor chip above the passive components, as required in claims 1 and 11 of the Applicants' invention.

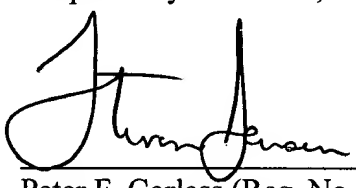
Richman fails to remedy the deficiencies of the Marrs reference. Richman also fails to teach or suggest a semiconductor package or fabricating method in which a plurality of passive devices are encapsulated and a semiconductor chip is disposed above the passive devices. In

Richman, a chip 25 (or other active/passive component) is attached to a mounting pad 22, and wires 23 electrically connect the chip 25 to internal fingers 21.1 (see FIG. 2, as cited in the Office Action). However, there is no teaching or suggestion in Richman for disposing a semiconductor chip above passive devices, as required in claims 1 and 11 of the Applicants' invention.

As discussed above, neither Marrs nor Richman teach or suggest encapsulating a plurality of passive devices and disposing a semiconductor chip above the passive devices. Therefore, the combination of Marrs in view of Richman cannot anticipate or otherwise render obvious the Applicant's claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 5, 6, 15, and 16 have been amended as follows:

5. (Amended) The fabricating method of claim 1, wherein the insulative material is a thermosetting or thermoplastic material [such as] selected from the group consisting of epoxy, silicone [or] and polyimide.

6. (Amended) The fabricating method of claim [1] 3, wherein the insulative material completely encapsulates the top surfaces and [periphery] peripheries of the passive devices through a dispensing process.

15. (Amended) The semiconductor package of claim 11, wherein the insulative material is a thermosetting or thermoplastic material [such as] selected from the group consisting of epoxy, silicone [or] and polyimide.

16. (Amended) The semiconductor package of claim [11] 13, wherein the insulative material completely encapsulates the top surfaces and [periphery] peripheries of the passive devices through a dispensing process.